What is claimed is:

1. A voltage-level converter comprising:

a static voltage-level converter; and

a split-level output circuit coupled to the static voltage-level converter.

2. The voltage-level converter of claim 1, wherein the static voltage-level converter comprises:

an input node, a first output node, and a second output node;

a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to the input node;

a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node; and

an inverter coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node.

3. The voltage level converter of claim 2, wherein the split-level output circuit comprises a plurality of insulated-gate field-effect transistors.

4. The voltage-level converter of claim 1, wherein the static voltage-level converter comprises a first output node and a second output node and the split-level output circuit comprises a first split-level input node, a second split-level input node, a split-level output node, a first insulated-gate field-effect transistor (FET) coupled to the first split-level input node and a second insulated-gate FET coupled to the second split-level input node, the first insulated-gate FET being connected in series with the second insulated-gate FET, the first insulated gate FET and the second insulated gate FET having a

common node coupled to the split-level output node and the first split-level input node coupled to the first output node and the second split-level input node coupled to the second output node.

5. The voltage-level converter of claim 4, wherein the first insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect transistor.

6. The voltage-level converter of claim 5, wherein the second insulated-gate field-effect transistor comprises an n-type insulated gate field-effect transistor.

7. A voltage-level converter comprising:

a static voltage-level converter including an input node, a first pull-up node, a second pull-up node, an inverter output node, and an output node;

a first transistor coupled to the input node and the first pull-up node; and

a second transistor coupled to the second pull-up node and the inverter output node.

8. The voltage-level converter of claim 7, wherein the first transistor comprises an insulated gate field-effect transistor and the second transistor comprises an insulated-gate field-effect transistor.

9. The voltage-level converter of claim 7, wherein the first transistor comprises a p-type insulated-gate field-effect transistor and the second transistor comprises a p-type insulated-gate field-effect transistor.

10. The voltage-level converter of claim 9, further comprising:

an inverter coupled to the output node.

11. The voltage-level converter of claim 10, wherein the inverter comprises:

a single-input inverter.

12. The voltage-level converter of claim 11, wherein the inverter comprises:

an n-type insulated-gate field-effect transistor coupled to the output node;

a first p-type insulated-gate field-effect transistor coupled to the inverter output node;

a second p-type insulated-gate field-effect transistor coupled to the static level converter, wherein the n-type insulated-gate field-effect transistor, the first p-type insulated-gate field-effect transistor, and the second p-type insulated-gate field-effect transistor are connected in series.

13. A voltage-level converter comprising:

a static voltage-level converter having an input node and an output node;

a first transistor coupled to the input node and the static voltage-level converter; and

a second transistor coupled to the static voltage-level converter.

14. The voltage-level converter of claim 13, wherein the first transistor comprises a p-type insulated-gate field-effect transistor.

15. The voltage-level converter of claim 14, wherein the second transistor comprises a p-type insulated-gate field-effect transistor.

16. The voltage-level converter of claim 15, further comprising:

an inverter coupled to the output node.

17. The voltage-level converter of claim 16, wherein the inverter comprises a single-input inverter.

18. The voltage-level converter of claim 16, wherein the inverter comprises:

a multiple-input inverter coupled to at least three outputs of the static voltage-level converter.

19. A voltage-level converter comprising:

a static voltage-level converter comprising an input node, an output node, a first pair of serially connected transistors, a second pair of serially connected transistors, and an inverter coupled between the first pair of serially connected transistors and the second pair of serially connected transistors;

a first transistor located between the first pair of serially connected transistors and coupled to the input node; and

a second transistor located between the second pair of serially connected transistors and coupled to the inverter.

20. The voltage-level converter of claim 19, wherein the first transistor comprises an insulated-gate field-effect transistor.

21. The voltage-level converter of claim 20, wherein the second transistor comprises an insulated-gate field-effect transistor.

22. The voltage-level converter of claim 21, further comprising:

a buffer coupled to the output node.

23. The voltage-level converter of claim 22, wherein the buffer comprises a single-input inverter.

24. The voltage-level converter of claim 22, wherein the buffer comprises:

a multiple-input inverter coupled to at least three outputs of the static voltage-level converter.

25. The voltage-level converter of claim 24, wherein the multiple-input inverter has an inverter output node and comprises:

an n-type insulated-gate field-effect transistor;

a first p-type insulated-gate field-effect transistor; and

a second p-type insulated-gate field-effect transistor, wherein the n-type insulated-gate field-effect transistor, the first p-type insulated-gate field-effect transistor, and the second p-type insulated-gate field-effect are connected in series and the n-type insulated-gate field-effect transistor is coupled to the inverter output node, the first p-type insulated-gate field-effect transistor is coupled to the first pair of serially connected transistors, and the second p-type insulated-gate field-effect transistor is coupled to the inverter output node.

26. A logic unit comprising:

one or more first logic units adapted to operate at a first voltage;

one or more second logic units adapted to operate at a second voltage, the second voltage being greater than the first voltage; and

a voltage-level converter for coupling at least one of the one or more first logic units to at least one of the one or more second logic units, the voltage-level converter comprising:

a first voltage-level converter comprising an input node coupled to the at least one of the one or more first logic units, an output node coupled to the at least one of the one or more second logic units, an inverter output node, a first pair of serially connected transistors, and a second pair of serially connected transistors; and

a first transistor located between the first pair of serially connected transistors and coupled to the input node; and

a second transistor located between the second pair of serially connected transistors and coupled to the inverter output node.

27. The voltage-level converter of claim 26, wherein the first transistor comprises a first insulated-gate field-effect transistor and the second transistor comprises a second insulated-gate field-effect transistor.

28. The voltage-level converter of claim 27, wherein the first insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect transistor and the second insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect transistor.

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